REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 1-7, 9-32 and 37-39 are pending in the application. The Examiner additionally stated that claims 1-7, 9-32 and 37-39 are rejected. By this amendment, claims 28, 37-39 have been cancelled and claims 1, 27, 30 have been amended. Hence, claims 1-7, 9-27, and 29-32 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Claims

Rejections Under 35 U.S.C. §112

The Examiner rejected claims 1-7, 9 and 22 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which application regards as the invention.

More specifically, the examiner indicated that it is unclear how, in claim 1, an interrupt register, which is a physical object, is connected to a vector table, which is a data structure. Applicant respectfully traverses. Applicant does not know why the examiner has read a vector table as a data structure. Applicant submits that for the purposes of the present invention, he has described a vector table 422 as a register which stores vectors, just like the interrupt register stores interrupts. From paragraph [0039] applicant states:

> 418 provided by the PEVG 416. In addition, as will be further described below, the core 412 reads and writes values from/to particular registers within the status register 420, including a vector table 422, an interrupt register 424 (having a number of interrupt specific registers 426), and interrupt priority registers 428. In

Thus, the vector table 422 is defined as one of the particular registers within the status register 420 and is thus a physical object. For this reason, applicant respectfully requests the examiner to withdraw his rejection of this claim.

With respect to claim 22, the examiner stated that it is unclear if the priorities of the first interrupts established by the interrupt controller are the same as the architecturally fixed interrupt priorities of Claim 10. Applicant respectfully suggests that they may be, but they may be overridden by priorities programmed into the priority encoder. Applicant directs the examiner's attention to paragraph [0040] of the specification where two embodiments of the invention are described. In one embodiment, the priority for interrupts I0-I7 are architecturally defined. In an alternative embodiment, registers 428 are provided for each of the interrupt fields 426 to allow a system designer to create interrupt priority schemes according to their desire. Thus, priorities may be programmed, which match, or differ from those that are architecturally defined, or which provide for programming of priorities whether or not they have already been architecturally defined.

The examiner further stated that it is unclear how an architecturally fixed interrupt priority can be established by an interrupt controller. One skilled in the art will appreciate that such is typically accomplished based on which interrupt is physically coupled to which interrupt input on an interrupt controller, although other designs are possible.

For these reasons, Applicant respectfully requests the examiner to withdraw his rejection of claim 22.

Rejections Under 35 U.S.C. §102(b)

The Examiner rejected claim 10 under 35 U.S.C. 102(b) as being clearly anticipated by Motorola MCF 5206 Integrated Microprocessor as described in Freescale Semiconductor, Inc. Product Brief "MCF5206 Integrated Microprocessor" (hereinafter, MCF5206) and Freescale Semiconductor, Inc. "Addendum to MCF5206 User Manual" (hereinafter, MCF5206 Addendum). Applicant believes the Examiner intended to also reject claims 11-14, 16-17, 20-24, 27, and 29-30 because he provided rejection language in the office action, but forgot to indicate such rejection in his paragraph 6. Applicant respectfully traverses the Examiner's rejections.

Before dealing specifically with claim 10, Applicant would like to point out what the Interrupt Controller of MCF5206 teaches. More specifically, on page 5, MCF5206 states:

> **Interrupt Controller.** The interrupt controller provides user-programmable control of 3 or 7 external interrupt and 5 internal peripheral interrupts. Users can program each internal interrupt to any one of 7 interrupt levels and 4 priority levels within each of these levels. The 3 external interrupt signals can be configured as either fixed interrupt levels 1, 4, and 7, or as a 7-level encoded interrupt. Users can program the external interrupts to any one of the 4 priority levels within the respective interrupt levels.

There are two types of interrupts that are dealt with by the Interrupt Controller of MCF5206: 1) External interrupts (3 or 7); and 2) internal peripheral interrupts. The external interrupts appear to be interrupts IRQ1, 4, and 7, having interrupt priorities of IPL0, 1 and 2 respectively. The internal interrupts appear to be interrupts from peripheral modules such as the clock, the jtag, the dram controller, etc. All of these are HARDWARE generated interrupts occurring EXTERNAL to the coldfire core. That is, even though the internal interrupts are designated "internal", what is meant is that they are internal to the MCF5206 Integrated Microprocessor. What is NOT meant, is that any of the interrupts are generated by the processor core. Applicant has searched the MCF5206 reference and has not found any teaching, hint or suggestion to indicate programmability of core generated interrupts. Applicant respectfully suggests that what is taught by MCF5206 was actually described as prior art with respect to Figure 1, wherein interrupts 114 (Figure 1 of applicant's specification) are referred to as system interrupts (like MCF5206's internal interrupts), and interrupts 118 are referred to as external interrupts. Applicant suggests that what the examiner has found in MCF5206 is exactly what applicant has described as prior art.

For ease of reference, claim 10 is repeated below:

10. A microprocessor for handling interrupts, the microprocessor receiving first interrupts from an interrupt controller, the first interrupts having architecturally fixed interrupt priorities, the microprocessor comprising:

a core, for executing instructions, said core generating second interrupts;

priority storage logic coupled to said core, for storing programmable priorities for said second interrupts; and

a priority encoder, coupled to said core, and to said priority storage logic, for receiving the first and said second interrupts, and for prioritizing the first and said second interrupts utilizing the architecturally fixed interrupt priorities for the first interrupts, and said programmable priorities stored in said priority storage logic for said second interrupts.

Claim 10 particularly recites: 1) a core ... said core generating second interrupts; and 2) a priority encoder ... for prioritizing ... said second interrupts. Applicant respectfully suggests that the ability to provide programmable priority to core generated interrupts is novel, and is nowhere taught, suggested, or even hinted at by MCF5206. For all of the above reasons, applicant respectfully requests the examiner to withdraw his rejection of this claim.

With respect to claims 11, 12, 13, 14, 16, 17, 20, 21, 22, 23, and 24, these depend either directly or indirectly from claim 10 and add further limitations that are neither anticipated nor obviated by MCF5206, taken alone or in combination with MCF5206 Addendum. For the reasons stated above with respect to claim 10, applicant respectfully requests the examiner to withdraw his rejection of these claims.

The examiner rejected claim 27 for the same reasons as that of claim 10. Applicant respectfully suggests that claim 27 (as amended) specifically clarifies and recites a method for prioritizing off-core interrupts and core generated interrupts. As mentioned above, nothing in MCF5206, taken alone or in combination with MCF5206 Addendum, teaches, suggests, or even hints at prioritization of programmable priorities for core generated interrupts. For this reason, and for those listed above with respect to claim 10, Applicant respectfully requests the examiner to withdraw his rejection of this claim.

With respect to claims 29 and 30, these depend from claim 27 and add further limitations that are neither anticipated nor obviated by MCF5206, taken alone or in combination with

MCF5206 Addendum. For the reasons stated above with respect to claims 10 and 27, Applicant respectfully requests the examiner withdraw his rejection of these claims.

Rejections Under 35 U.S.C. §103(a)

The Examiner rejected claims 1 under 35 U.S.C. 103(a) as being unpatentable over MCF5206 and MCF5206 Addendum, in view of U.S. Patent No. 6,499,078 to Beckert et al. (hereinafter Beckert). Applicant believes that the examiner intended on also rejected claims 2, 4, 5, 6, 7 and 9, but forgot to reference these in his paragraph 23. Applicant respectfully traverses the Examiner's rejections.

With respect to claim 1, it is repeated below as amended for ease of reference:

1. A processing system comprising:

a plurality of first interrupts generated by a core, said plurality of first interrupts having programmable priorities;

a plurality of second interrupts that are generated external to said core, said second interrupts having architecturally fixed interrupt priorities;

a status register, coupled to said core, said status register comprising a vector table, and an interrupt register, said interrupt register having a plurality of configurable priority registers for storing said programmable priorities; and

a priority encoder, coupled to both said first interrupts and to said second interrupts, and to said status register, said priority encoder prioritizing said first and second pluralities of interrupts utilizing said programmable priorities for said first interrupts and said architecturally fixed interrupt priorities for said second interrupts.

As mentioned above with respect to claim 10, nothing in MCF5206 and MCF5206 Addendum, deals with core generated interrupts or programmable priorities for core

generated interrupts. Applicant specifically claimed first interrupts "generated by a core". See Figure 4, lines 414. Also see the prior art as described with respect to Figure 1 and referenced in paragraph [0004]. What does a core do? Among other things, the core 104 executes instructions. Such a core also generates interrupts (e.g., divide by zero). Nothing in MCF5206 or MCF5206 Addendum deals with interrupts generated by the core, much less programmability of priority of such core generated interrupts. Adding the reference to Beckert to deal with a status register does nothing to teach, suggest, or even hint at providing programmable priorities for core generated interrupts. For these reasons, and all those stated above with respect to claims 10 and 27, applicant respectfully requests the examiner withdraw his rejection of claim 1.

With respect to claims 2, 4, 5, 6, 7, and 9, these depend either directly or indirectly from claim 1 and add further limitations which are neither anticipated nor obviated by MCF5206, taken alone or in combination with either or both of MCF5206 Addendum and/or Beckert. For the reasons stated above with respect to claim 1, applicant respectfully requests the examiner withdraw his rejection of these claims.

The examiner rejected claim 3 as being unpatentable over MCF5206, MCF5206 Addendum, and Beckert, and further in view of US Patent No. 5,788,500 to Agrawal et al. The examiner cites Agrawal because he teaches the use of a performance counter interrupt. However, Agrawal does not teach programmable priority of core generated interrupts. Since MCF5206, MCF5206 Addendum, and Beckert fail to teach such, adding Agrawal does not teach programmable priority of core generated interrupts. For all of the reasons stated above with respect to claims 1, 10 and 27, applicant respectfully requests the examiner to withdraw his rejection of this claim.

The examiner rejected claims 15 and 28 as being unpatentable over MCF5206, MCF5206 Addendum and further in view of Agrawal. Claim 15 depends from claim 10 and adds further limitations that are neither anticipated nor obviated by the combination referenced by the examiner. For all of the reasons stated above with respect to claim 10, applicant respectfully requests the examiner to withdraw his rejection of claim 15. With respect to claim 28, it has been cancelled thereby rendering this rejection moot.

The examiner further rejected claims 18 and 19 as being unpatentable over MCF5206 further in view of U.S. Patent No. 5,148,544 to Cutler. Cutler teaches a register storing information related to an interrupt condition accessible during privileged mode. However, Cutler does not teach programmable prioritization of core generated interrupts. For this reason, and for those listed above with respect to claim 10, applicant respectfully requests the examiner to withdraw his rejection of these claims.

The examiner further rejected claims 25, 26, 31 and 32 as being unpatentable over MCF5206 and further in view of U.S. Patent No. 5,940,587 to Zimmer. Zimmer teaches programmable offset storage means to produce an interrupt vector. However, Zimmer does not teach programmable prioritization of core generated interrupts. For all of the reasons stated above, applicant respectfully requests the examiner to withdraw his rejection of these claims.

Rejections Under 35 U.S.C. §101

The Examiner rejected claims 37-39 because the claimed invention is directed at non-statutory subject matter. Applicant disagrees with the current position of the patent office with respect to such claims, and believes that the PTO's current position with respect to such claims is nowhere found in case law or legislation. However, to further advance this case towards allowance, applicant has cancelled claims 37-39.

CONCLUSIONS

In view of the arguments advance above, Applicant respectfully submits that claims 1-7, 9-27, 29-32 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

I hereby certify under 37 CFR 1.8 that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date of signature shown below.

Respectfully submitted,
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3/19/06
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